12-27-99

A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application		PATENT APPLICATION
Inventor(s):	Dove, et al.	
SC/Serial No.:	Unknown	
Filed:	Herewith	
Title:	STACKPLANE ARCHITECTURE	

CERTIFICATE OF MAILING BY "EXPRESS MAIL"
UNDER 37 C.F.R. §1.10

"Express Mail" mailing label number: EL080529871US
Date of Mailing: December 22, 1999

I hereby certify that this correspondence is being deposited with the United States Postal Service, utilizing the "Express Mail Post Office to Addressee" service addressed to Box **PATENT APPLICATION, Assistant Commissioner for Patents, Washington, DC 20231** and mailed on the above Date of Mailing with the above "Express Mail" mailing label number.

Matthew A. Mahling (Signature)
Matthew A. Mahling
Signature Date: December 22, 1999

UTILITY PATENT APPLICATION TRANSMITTAL LETTER UNDER 37 C.F.R §1.53(b)

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Transmitted herewith for filing is the patent application identified as follows:

Inventor(s): Jason W. Dove and Paul Franceschini

Title: STACKPLANE ARCHITECTURE

No. of pages in Specification: 40 ; No. of Claims: 56 .

No. of Sheets of Drawings: 6 ; Formal: __, Informal: X .

Attorney Docket No.:DSCC1067WSW/LAH
lah/dscc/1067.005

105.001:05/06/99
12/21/99-10:28

Also enclosed are:

X A Declaration.

X An Assignment and Recordation Form Cover Sheet.

__ A certified copy of a priority application.

__ A Power of Attorney.

__ A Statement Claiming Small Entity Status.

__ An Information Disclosure Statement under 37 C.F.R. §1.56.

The filing fee pursuant to 37 C.F.R. §1.16 is determined as follows:

	No. Filed		No. Extra		Rate Small Entity/ Other Than Small Entity		
Basic Fee					$380.00 $760.00	=	$760.00
Total Claims	56 - 20	=	36 *	X	$ 9.00 $ 18.00	=	$648.00
Independent Claims	4 - 3	=	1 *	X	$ 39.00 $ 78.00	=	$ 78.00
First Presentation of Multiple Dependent Claim(s)	__				$130.00 $260.00	=	$
					Total	=	$1486.00

*If the difference is less than zero, enter "0".

__ Please charge Deposit Account No. 06-1325 in the amount of $____. A duplicate copy of this authorization is enclosed.

X A check in the amount of $ 1526.00 to cover the filing fee ($ 1486.00), and assignment recording fee ($40.00), if applicable, is enclosed.

_X_ The Commissioner is hereby authorized to charge underpayment of any additional fees (including those listed below) or credit any overpayment associated with this communication to Deposit Account No. 06-1325. A duplicate copy of this authorization is enclosed.

_X_ Any additional filing fees under 37 C.F.R. §1.16.

_X_ Any patent application processing fees under 37 C.F.R. §1.17.

This application is filed pursuant to 37 C.F.R. §1.53(b) in the name of the above-identified Inventor(s).

___ This application claims priority to an earlier-filed Provisional patent application, as set forth more fully in this application.

Please direct all correspondence concerning the above-identified application to the following address:

ALCATEL USA
1000 Coit Road, MS LEGL2
Plano, TX 75075

Respectfully submitted,

Date: 12/22/99

By: _____
Warren S. Wolfeld
Reg. No. 31,454

FLIESLER, DUBB, MEYER & LOVEJOY LLP
Four Embarcadero Center, Suite 400
San Francisco, California 94111-4156
Telephone: (415) 362-3800

Separator Sheet

AAA

Application Text

Place Papers behind this sheet in the following order:

- ...ary Amendment
- ...ion (English Language Only)

STACKPLANE ARCHITECTURE

Inventors:

Jason W. Dove
Paul Franceschini

Attorney Docket No.: DSCC01067WSW/LAH
/lah/dscc/1067.001

Client Ref.: 1067-00

Express Mail No: EL080529871 05

STACKPLANE ARCHITECTURE

Inventors:

Jason W. Dove
Paul Franceschini

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to telecommunications, and more particularly, to a telecommunications switching network.

2. Background

The telecommunications industry has developed telecommunications switching systems including channel banks with cross-connections to establish communication links. A plurality of channel banks are typically provided on a standard equipment rack to serve as a node in a telecommunications switching network. A plurality of such nodes may be formed with point-to-point, ring or branch interconnections, or a combination thereof, to form a telecommunications switching network. However, conventional channel banks within each node are connected through interfaces with limited bandwidths. Furthermore, the scalability of conventional channel banks in a telecommunications node is limited.

Therefore, there is a need for a scalable and modular digital loop carrier system with integrated transport, switching and control functions which can be flexibly expanded to increase its transport capacity. Furthermore, there is a need for interfaces between the channel banks with increased bandwidths which allow simultaneous transfer of different native mode traffic types, including time division multiplex (TDM) and asynchronous transfer mode (ATM) traffic.

SUMMARY OF THE INVENTION

In accordance with the present invention, a scalable digital loop carrier system roughly comprises:

(a) a primary channel bank;

(b) an asynchronous transfer mode (ATM) interface connected to the primary channel bank;

(c) a time division multiplex (TDM) interface connected to the primary channel bank; and

(d) at least a first secondary channel bank connected to the primary channel bank through the ATM and TDM interfaces, the primary channel bank capable of providing clock synchronization to the secondary channel bank, wherein the primary channel bank and the secondary channel bank each comprise:

(i) a time slot cross-connect interchanger (TSI) having a plurality of subscriber bus interfaces; and

(ii) an ATM access controller connected to the TSI, the ATM access controller having a plurality of ATM cell bus interfaces.

In an embodiment, the primary channel bank further comprises a synchronous transport signal (STS) cross-connect controller connected to the TSI and the ATM access controller in the primary channel bank. In a further embodiment, the primary channel bank further comprises a synchronous optical network (SONET) framer connected to the STS cross-connect controller in the primary channel bank. In an embodiment, the system further comprises a plurality of STS transport cards connected to the STS cross-connect controller in the primary channel bank.

In an embodiment, the secondary channel bank also comprises an STS cross-connect controller connected to the TSI and the ATM access controller in the secondary channel bank. In a further embodiment, the secondary channel bank further comprises a SONET framer connected to the STS cross-connect controller in the secondary channel bank. In an embodiment, the system further comprises a plurality of STS transport cards connected

to the STS cross-connect controller in the secondary channel bank.

In an embodiment, the TDM interface is capable of providing a plurality of STS-1 channels in a SONET frame. In an embodiment, the primary channel bank further comprises a timing generator to provide timing reference to the TSI and the ATM access controller in the primary channel bank. In an embodiment, the timing generator has a timing reference input and a clock synchronization output connected to the secondary channel bank. In a further embodiment, the secondary channel bank further comprises a timing generator to provide timing reference to the TSI and the ATM access controller in the secondary channel bank. In a further embodiment, the timing generator in the secondary channel bank is synchronized by a clock synchronization signal received from the clock synchronization output of the primary channel bank.

In an embodiment, a plurality of secondary channel banks are connected to the primary channel bank in a daisy-chain configuration. Each of the primary and secondary channel banks may be connected directly to two secondary channel banks. The primary channel bank may be connected to two secondary channel banks, and additional secondary channel banks may be connected to the primary channel bank through intermediary secondary

channel banks. The TDM and ATM interfaces provide TDM and ATM data link channels for transferring narrowband and broadband data between the channel banks in the scalable digital loop carrier system.

Advantageously, the digital loop carrier system according to the present invention allows flexible expansion of the channel banks to increase the transport capacity of the digital loop carrier system in a modular configuration. Furthermore, the TDM and ATM interfaces between the channel banks are capable of providing an increased total bandwidth which allows simultaneous transfer of different native mode traffic types including TDM, STS, and ATM traffic.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described with respect to particular embodiments thereof, and references will be made to the drawings in which:

FIG. 1 shows a block diagram of an embodiment of a scalable digital loop carrier system according to the present invention;

FIG. 2 shows a block diagram of an embodiment of timing and synchronization for the primary and secondary channel banks in the scalable digital loop carrier system according to the present invention;

FIG. 3 shows a block diagram of an embodiment of the primary and secondary channel banks in the scalable digital loop carrier system according to the present invention with time slot cross-connect interchangers (TSI) and asynchronous transfer mode (ATM) access controllers;

FIG. 4 shows a block diagram of an embodiment of the primary and secondary channel banks in the scalable digital loop carrier system according to the present invention with TSI and ATM access controllers and synchronous transport signal (STS) cross-connect controllers connected to a plurality of STS transport cards;

FIG. 5 shows a block diagram of an embodiment of the scalable digital loop carrier system according to the present invention in a daisy-chain configuration;

FIG. 6 shows a block diagram of an embodiment of a node control processor (NCP) for stackplane access control in the scalable digital loop carrier system according to the present invention;

FIG. 7 shows a block diagram illustrating a copper wired time division multiplex (TDM) payload path in an embodiment of the scalable digital loop carrier system according to the present invention; and

FIG. 8 shows a block diagram illustrating a synchronous optical network (SONET) TDM payload path in

an embodiment of the scalable digital loop carrier system according to the present invention.

DETAILED DESCRIPTION

FIG. 1 shows a block diagram of a scalable digital loop carrier system in a communications network node in an embodiment according to the present invention. A plurality of such communications network nodes may be provided in a data network with point-to-point, linear chain, ring or branch interconnections, or a combination thereof, between the nodes. The scalable digital loop carrier system as shown in FIG. 1 may also be implemented on a single common equipment rack 10 and used as a stand-alone communications switching network.

As shown in FIG. 1, the scalable digital loop carrier system comprises a primary channel bank 2 and a plurality of secondary channel banks 4a, 4b, 4c, . . . 4h. In an embodiment, the primary and secondary channel banks in the digital loop carrier system are installed on different levels of a common equipment rack, with physical stackplanes between adjacent channel banks on the common equipment rack 10. Asynchronous transfer mode (ATM) and time division multiplex (TDM) interfaces are installed on the stackplane as a physical layer transceiver which provides ATM and TDM data link channels between the

channel banks. In the embodiment shown in FIG. 1, an ATM stackplane interface 6 and a TDM stackplane interface 8 are shown as separate interfaces on the stackplane. In an embodiment, each physical stackplane between two adjacent channel banks on the common equipment rack 10 provides both ATM and TDM interfaces for ATM and TDM channel interconnections between the adjacent channel banks.

In an embodiment, the primary channel bank 2 in the scalable digital loop carrier system according to the present invention is connected to one or more network management interfaces 12 and one or more network transport interfaces 14 which control node-to-node traffic flow in a data communications network formed by a plurality of such nodes. The primary channel bank 2 and each of the secondary channel banks 4a, 4b, 4c, . . 4h provide a plurality of subscriber interfaces which are capable of communicating with a plurality of transport cards, including plain old telephone service (POTS) subscriber service cards.

In the embodiment shown in FIG. 1, the primary channel bank 2 and the secondary channel banks 4a, 4b, 4c, . . 4h are connected through the stackplane interfaces in a linear chain configuration. Each of the channel banks is connected to adjacent upper and lower channel banks through stackplanes between the

channel banks, except for the secondary channel bank 4h at the top and the secondary channel bank 4d at the bottom of the common equipment rack 10.

The scalable digital loop carrier system according to the present invention is expandable if necessary to accommodate higher capacity TDM or ATM traffic or to increase the number of subscriber interfaces provided by each communications node. In an embodiment in which the physical size of the common equipment rack 10 is not a limitation, additional secondary channel banks may be connected to the secondary channel banks 4d and 4h as shown in FIG. 1 through additional ATM and TDM stackplane interfaces if necessary to increase the transport capacity of the digital loop carrier system.

FIG. 2 shows a block diagram illustrating the provision of timing references for a digital loop carrier system in an embodiment according to the present invention. In an embodiment, the primary channel bank 2 provides timing and synchronization to all of the secondary channel banks, including secondary channel banks 4a and 4e. In FIG. 2, a stackplane immediately above a given one of the channel banks is denoted as a "north" stackplane, whereas the stackplane immediately below the given channel bank is denoted as a "south" stackplane for the purpose of simplifying the description.

In an embodiment, the primary channel bank 2 comprises a timing generator 16 to provide a timing reference for the ATM and TDM interface functions as well as cross-connect functions within the primary channel bank 2. In a further embodiment, the timing generator 16 in the primary channel bank 2 has a node timing reference input 18 and a clock synchronization output 20, which is connected to all of the secondary channel banks including the secondary channel banks 4a and 4e in the scalable digital loop carrier system. The primary channel bank 2 provides a clock synchronization signal through the clock synchronization output 20 for synchronizing the clocks in the secondary channel banks.

In an embodiment, the timing reference input 18 for the timing generator 16 in the primary channel bank 2 comprises a synchronous optical network (SONET) timing reference input provided over the SONET. In another embodiment, the node timing reference input 18 for the timing generator 16 in the primary channel bank 2 comprises a T1 timing reference input if the scalable digital loop carrier system according to the present invention is used for transporting T1 communications payload. In yet another embodiment, the node timing reference input 18 for the timing generator 16 in the primary channel bank 2 comprises a building integrated

timing supply (BITS) input which is provided by an office BITS clock in a typical telephone switching system.

In an embodiment, the secondary channel banks each comprise a timing generator to provide a timing reference for the TDM and ATM functions as well as cross-connect functions within the respective secondary channel bank. For example, the secondary channel bank 4a immediately below the primary channel bank 2 includes a timing generator 20 while the secondary channel bank 4e immediately above the primary channel bank 2 includes another timing generator 22. In an embodiment, the timing generator in each of the secondary channel banks is synchronized by the clock synchronization signal which is received from the clock synchronization output 20 of the timing generator 16 of the primary channel bank 2.

In an embodiment, the timing reference for the timing generators 20 and 22 in the secondary channel banks 4a and 4e are provided from the stackplanes which are connected to the primary channel bank 2, whereas the timing reference for the timing generator 16 in the primary channel bank 2 is provided from an external source, such as a bits, SONET, or T1 clock. For the purpose of simplified illustration, signal paths for the clock synchronization signals transferred between

the primary and secondary channel banks in southbound and northbound directions are shown as separate clock channels 24 and 26, respectively, between the channel banks in FIG. 2. In an embodiment, the timing generators 20 and 22 in the secondary channel banks 4a and 4e provide timing feedbacks along respective return paths to the controlling timing generator 16 in the primary channel bank 2. Feedback loops between the timing generators in the primary and secondary channel banks allow timing and synchronization to be stabilized for each of the timing generators in the primary and secondary channel banks.

FIG. 3 shows a block diagram of an embodiment of a scalable digital loop carrier system according to the present invention in which each of the channel banks comprises a time slot cross-connect interchanger (TSI) and an ATM access controller. In FIG. 3, the primary channel bank 2 comprises a TSI 28 and an ATM access controller 30 while the secondary channel bank 4a comprises another TSI 32 and another ATM access controller 34. In an embodiment, other secondary channel banks in the scalable digital loop carrier system according to the present invention have configurations similar to that of the secondary channel bank 4a as shown in FIG. 3.

In an embodiment, each TSI is capable of performing the function of cross-connecting any of the individual time slots on a subscriber bus interface to another time slot on another subscriber bus interface within the channel bank. In a further embodiment, each TSI also performs subscriber bus data link (SBDL) and signaling functions for the subscriber bus interfaces. In an embodiment, the TSI in each of the primary and secondary channel banks is capable of cross-connecting the time slots of a plurality of subscriber bus interfaces, such as variable rate subscriber bus interfaces as described in Patent Application Serial No. _____, titled "Variable Rate Subscriber Bus", filed _____, incorporated herein by reference.

Referring to FIG. 3, the primary channel bank 2 further comprises a synchronous transport signal (STS) cross-connect controller 36 which is connected to the TSI 28 in the primary channel bank 2. The STS cross-connect controller 36 uses an STS channel format to pass STS traffic between the channel banks. In an embodiment, the STS cross-connect controller has 12 STS-1 buses which provide up to 12 STS-1 channels for each transport card slot connected to the STS cross-connect controller 36. In an embodiment, the STS-1 payload transported by the STS cross-connect controller

36 may be any virtual tributary (VT) grouping that complies with GR-253 standard.

The STS-1 payload transferred from the STS cross-connect controller 36 passes through the stackplane transparently between the primary and secondary channel banks. In an embodiment, the ATM access controller in each of the primary and secondary channel banks is connected to the TSI within the respective channel bank for time slot cross-connections. In an embodiment, each of the ATM access controllers 30 and 34 comprises an ATM switch fabric.

FIG. 4 shows a block diagram of an embodiment in which each of the primary and secondary channel banks further comprises an STS cross-connect controller for transporting STS-1 payloads between STS transport card slots and passing the STS-1 payloads through the stackplane transparently between different channel banks. As shown in FIG. 4, the secondary channel bank 4a further comprises an STS cross-connect controller 38 to provide a plurality of transport card slots for additional STS transport cards. In an embodiment, the STS cross-connect controllers 36 and 38 in the primary and secondary channel banks 2 and 4a each provide four STS transport card slots, each of which is capable of transporting up to 12 STS-1 signals. In FIG. 4, four STS transport cards 40a, 40b, 40c and 40d are connected

to the STS cross-connect controller 36 in the primary channel bank 2, while four additional STS transport cards 42a, 42b, 42c and 42d are connected to the STS cross-connect controller 38 in the secondary channel bank 4a.

In an embodiment, each of the STS transport cards is capable of supporting up to 12 STS-1 channels. Each of the STS cross-connect controllers 36 and 38 thus has a transport capacity of up to 48 STS-1 channels in four groups of 12 STS-1 channels in the embodiment shown in FIG. 4. In an embodiment, any group of 12 of the 48 STS-1 channels may be cross-connected to 16 TDM/STS channels provided by the TDM interface over the stackplane between the channel banks. In a further embodiment, the 12 STS-1 channels in any one of the four groups from the STS cross-connect controller are connected to the TDM/STS channels of the TDM interface over the stackplane by bit assignments in a TSI source pointer provided by the TSI within the respective channel bank.

In the embodiments described above, the stackplane between adjacent channel banks provides an interbank link for timing, payload and communications. In an embodiment, the stackplane provides transparent TDM, STS and ATM duplex data link channels. In an embodiment, the stackplane is organized as a single

physical layer transceiver that has two data links, namely, a TDM/STS data link and an ATM data link. In an embodiment, the TDM/STS data link consists of 16 time division multiplexed logical channels. In an embodiment, each of the logical channels in the TDM/STS data link is a 6.48 megabyte or 51.84 megabit channel. Each STS-1 channel is organized as 810 bytes per SONET frame which has a frame length of 125 μs. In an embodiment, the ATM data link is a single 103 megabit data link organized as a single 12960 byte, 125 μs frame that carries 216 ATM cells per frame.

FIG. 5 shows a block diagram of an embodiment in which the channel banks are organized in a redundant daisy-chain configuration. In this embodiment, the timing and synchronization for the secondary channel banks 4a, . . 4e, 4f, . . are provided by the primary channel bank 2. The stackplanes provide daisy-chains from the primary channel bank 2 in two directions, referred to as "north" and "south". The north of the secondary channel bank 4a is connected to the south of the primary channel bank 2. However, the north of the primary channel bank 2 is connected to the north of the secondary channel bank 4e in this arrangement. The north of the secondary channel bank 4f is connected to the south of the secondary channel bank 4e. The redundant daisy-chain configuration is simply a

variation of the linear chain configuration shown in FIG. 1. Although linear-chain and daisy-chain configurations for interconnections between channel banks have been described above, other configurations may also be provided for interconnections between the channel banks within the scope of the present invention.

FIG. 6 shows a block diagram of a node control processor (NCP) which incorporates TDM, STS and ATM transport functions and interbank transport control functions in each of the primary and secondary channel banks in the scalable digital loop carrier system according to the present invention. The NCP contains the basic electronics to support the channel bank in which the NCP is provided. In an embodiment, the NCP includes a microprocessor 44, a random access memory (RAM) 46, a flash memory 48, a data link and control tone card (DCT) 50 and one or more external interfaces such as an Ethernet interface or an RS-232 serial interface. In an embodiment, the NCP also includes a PCMCIA port 52 for optional peripheral equipment. A clock reference is provided to one or more timing generators 54 in the NCP to provide clock signals for various applications.

In an embodiment, the functions performed by the TSI 56, the ATM access controller or ATM switch 58, and

the STS cross-connect controller 60 in the channel bank are integrated in the NCP. The ATM switch 58 has a plurality of ATM cell bus interfaces for transporting ATM cells while the STS cross-connect controller 60 has a plurality of STS transport card slots for transporting STS-1 signals to a plurality of STS transport cards. In an embodiment, the STS cross-connect controller 60 has four transport card slots each capable of supporting up to 12 STS-1 channels.

The TSI 56 is connected to both the ATM switch 58 and the STS cross-connect controller 60. The TSI 56 has a plurality of subscriber bus interfaces and is capable of cross-connecting any time slot on one of the subscriber bus interfaces to another time slot on another one of the subscriber bus interfaces. In an embodiment, the TSI 56 is capable of cross-connecting the time slots of variable rate subscriber bus interfaces, an embodiment of which is described in Patent Application Serial No. _____, previously incorporated by reference.

In an embodiment, the node control processor as shown in FIG. 6 further comprises a SONET framer 62 connected to the STS cross-connect controller 60. In an embodiment in which TDM traffic is carried over the SONET, the STS-1 signals are framed by a standard SONET frame which has a duration of 125 μs. The TSI 56 is

connected to both the SONET framer 62 and the ATM switch 58 and is controlled by the microprocessor 44 to perform cross-connecting functions between the subscriber bus interfaces. The TSI 56 also controls the access of the SONET framer 62 to the stackplane with its source pointer memory. In an embodiment, the microprocessor 44 is connected to the TSI 56 through a processor bus in the NCP. The transport slots for the ATM switch 58 include high speed cell buses and the transport slots for the STS cross-connect controller 60 may be connected to a plurality of STS transport cards such as the STS transport cards 40a, 40b, 40c and 40d as shown in FIG. 4, each of which is capable of supporting up to 12 STS-1 channels.

FIG. 7 shows a block diagram illustrating a TDM payload path for copper wire transport in an embodiment of the scalable digital loop carrier system according to the present invention. In this embodiment, the POTS signals are cross-connected to a network service interface by a time slot cross-connect interchanger (TSI) 64 in the NCP 66. The network service interface may be either a copper wire network interface or an optical fiber network interface. Typical copper wire network service interfaces include digital signal 1 (DS1) and high-speed digital subscriber line (HDSL) interfaces which are provided for channel unit slots

68. Typical optical fiber network service interfaces such as optical carrier 3 (OC-3) and OC-12 are provided in transport slots 70.

A plurality of subscriber service cards 72 for carrying POTS traffic may be connected to the channel unit slots 68 which communicate with the TSI 64 over a subscriber bus interface. A plurality of network cards 74 for carrying quadruple HDSL traffic may be plugged into the transport slots 70 which communicate with the TSI 64 over another subscriber bus interface. In an embodiment, subscriber bus interfaces connecting the channel unit slots 68 and the transport slots 70 to the TSI 64 are variable rate subscriber buses described in Patent Application Serial No. _____, previously incorporated by reference.

The TSI 64 communicates with the stackplane 76 which provides a physical layer data link for TDM traffic as well as ATM traffic between channel banks. In the direction from the subscriber bus interfaces to the stackplane, the TSI 64 performs a sequential read of all of the time slots and stores them sequentially in a memory. Each location in the memory of the TSI 64 represents a subscriber bus interface time slot. In an embodiment, two such memories are provided within the TSI 64, one of which is used for reading data from the subscriber bus interfaces and another one of which is

used for writing the data to the stackplane 76. A source pointer is provided within the TSI 64 to address the memory for the time slots for writing operations to the stackplane. The TSI memory also includes one bit to indicate whether the data is to be written to the channel bank north of the stackplane and another bit to indicate whether the data is to be written to the channel bank south of the stackplane.

In the direction from the stackplane 76 to the channel unit slots 68 or to the transport slots 70, the data bytes from the stackplane 76 are read sequentially by the memory in the TSI 64 from the stackplane 76. The data bytes are stored sequentially in the TSI memory and read out of the memory by the subscriber bus interface using a memory source pointer. Sequential writing and random reading operations are performed in an embodiment to allow the data to be transferred from the stackplane 76 to the channel unit slots 68 and to the transport slots 70 in a broadcast mode.

FIG. 8 shows a block diagram illustrating a SONET TDM payload path in an embodiment of the scalable digital loop carrier system according to the present invention. In a manner similar to TDM data transport using copper wires, the POTS DS0 traffic is transferred between channel unit slots 78 and a TSI 80 over a

subscriber bus interface. The TSI 80, which is located in an NCP 82, combines a plurality of DS0 signals together to form a virtual tributary (VT) payload of 24 DS0 signals. In an embodiment, up to 28 such VT payloads can be placed into one of the 16 TDM channels on the stackplane 84. The VT payload, which is not in the VT format, is inserted into one of the 16 TDM channels on the stackplane by the TSI 80. In an embodiment, 28 VT payloads with a total of 672 DS0 signals are inserted into one of the stackplane TDM channels to form an STS-1.

TDM data received from the stackplane 84 are picked up by a SONET formatter 86, which converts the TDM payload into VT payloads and STS-1 signals. The STS-1 signals are cross-connected by a STS cross-connect controller 88, which passes the cross-connected STS-1 signals to a SONET transport card slot 90. A SONET network card may be plugged into the SONET transport card slot 90 to generate an OC-3 or OC-12 payload for SONET transportation. In an embodiment, a plurality of subscriber service cards 92 are plugged into the channel bank slots 78 for transferring DS0, DS1 or T1 signals over the subscriber bus interface, an embodiment of which is described in Patent Application Serial No. _____, previously incorporated by reference.

The stackplane architecture for the digital loop carrier system according to the present invention allows the system to be flexibly expanded with additional secondary channel banks as needed to increase the transport capacity of a communications node in a data network. Because both TDM and ATM interfaces are provided on the stackplane for linking the channel banks in the scalable digital loop carrier system, a variety of data formats including TDM, STS and ATM traffic are supported by the stackplane. The stackplane provides expanded bandwidth for different modes of native mode traffic types to allow the scalable digital loop carrier system according to the present invention to provide various types of communications including voice, video and data communications simultaneously.

The present invention has been described with respect to particular embodiments thereof, and numerous modifications can be made which are within the scope of the claims.

CLAIMS

What is claimed is:

1. A scalable digital loop carrier system capable of providing voice, video and data communications, the system comprising:

(a) a primary channel bank;

(b) an asynchronous transfer mode (ATM) interface connected to the primary channel bank;

(c) a time division multiplex (TDM) interface connected to the primary channel bank; and

(d) at least a first secondary channel bank connected to the primary channel bank through the ATM and TDM interfaces, the primary channel bank capable of providing clock synchronization to the secondary channel bank, wherein the primary channel bank and the secondary channel bank each comprise:

(i) a time slot cross-connect interchanger (TSI) having a plurality of subscriber bus interfaces; and

(ii) an ATM access controller connected to the TSI, the ATM access controller having a plurality of ATM cell bus interfaces.

2. The system of claim 1, wherein the primary channel bank further comprises a synchronous transport signal (STS) cross-connect controller connected to the TSI in the primary channel bank.

3. The system of claim 2, wherein the primary channel bank further comprises a synchronous optical network (SONET) framer connected to the STS cross-connect controller in the primary channel bank.

4. The system of claim 2, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the primary channel bank.

5. The system of claim 1, wherein the secondary channel bank further comprises a synchronous transport signal (STS) cross-connect controller connected to the TSI in the secondary channel bank.

6. The system of claim 5, wherein the secondary channel bank further comprises a synchronous optical

network (SONET) framer connected to the STS cross-connect controller in the secondary channel bank.

7. The system of claim 5, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the secondary channel bank.

8. The system of claim 1, wherein the TDM interface is capable of supporting 16 time division multiplexed channels.

9. The system of claim 1, wherein the ATM interface is capable of transporting 216 ATM cells per 125 μs frame.

10. The system of claim 1, wherein the TDM interface is capable of providing a plurality of synchronous transport signal-one (STS-1) channels in a synchronous optical network (SONET) frame.

11. The system of claim 1, wherein the primary channel bank further comprises a timing generator to provide timing reference to the TSI and ATM access controllers in the primary channel bank, the timing generator having a timing reference input and a clock

synchronization output connected to the secondary channel bank.

12. The system of claim 11, wherein the timing reference input comprises a synchronous optical network (SONET) timing reference input.

13. The system of claim 11, wherein the timing reference input comprises a T1 timing reference input.

14. The system of claim 11, wherein the timing reference input comprises a building integrated timing supply (BITS) input.

15. The system of claim 11, wherein the secondary channel bank further comprises a timing generator to provide timing reference to the TSI and the ATM access controller in the secondary channel bank, the timing generator in the secondary channel bank synchronized by a clock synchronization signal received from the clock synchronization output of the primary channel bank.

16. The system of claim 1, further comprising a second secondary channel bank connected to the primary channel bank through the TDM and ATM interfaces.

17. The system of claim 16, wherein the second secondary channel bank is connected to the first secondary channel bank through the TDM and ATM interfaces.

18. A scalable digital loop carrier system capable of providing voice, video and data communications, the system comprising:

(a) a primary channel bank;

(b) an asynchronous transfer mode (ATM) interface connected to the primary channel bank;

(c) a time division multiplex (TDM) interface connected to the primary channel bank; and

(d) at least a first secondary channel bank connected to the primary channel bank through the ATM and TDM interfaces, the primary channel bank capable of providing clock synchronization to the secondary channel bank, wherein the primary channel bank and the secondary channel bank comprise respective node control processors capable of communicating to each other, each of the node control processors comprising:

(i) a time slot cross-connect interchanger (TSI) having a plurality of subscriber bus interfaces;

(ii) an ATM access controller connected to the TSI, the ATM access controller having a plurality of ATM cell bus interfaces;

(iii) a synchronous transport signal (STS) cross-connect controller connected to the TSI; and

(iv) a synchronous optical network (SONET) framer connected to the STS cross-connect controller.

19. The system of claim 18, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the primary channel bank.

20. The system of claim 18, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the secondary channel bank.

21. The system of claim 18, wherein the STS cross-connect controller is capable of supporting at least 12 STS-1 channels.

22. The system of claim 18, wherein the TDM interface is capable of providing a plurality of synchronous transport signal-one (STS-1) channels in a synchronous optical network (SONET) frame.

23. The system of claim 18, wherein the primary channel bank further comprises a timing generator to provide timing reference to the TSI and the ATM access controller in the primary channel bank, the timing generator having a timing reference input and a clock synchronization output connected to the secondary channel bank.

24. The system of claim 23, wherein the timing reference input comprises a synchronous optical network (SONET) timing reference input.

25. The system of claim 23, wherein the timing reference input comprises a T1 timing reference input.

26. The system of claim 23, wherein the timing reference input comprises a building integrated timing supply (BITS) input.

27. The system of claim 23, wherein the secondary channel bank further comprises a timing generator to provide timing reference to the TSI, the STS cross-connect controller and the ATM access controller in the secondary channel bank, the timing generator in the secondary channel bank synchronized by a clock synchronization signal received from the clock synchronization output of the primary channel bank.

28. The system of claim 18, further comprising a second secondary channel bank connected to the primary channel bank through the TDM and ATM interfaces.

29. The system of claim 28, wherein the second secondary channel bank is connected to the first secondary channel bank through the TDM and ATM interfaces.

30. The system of claim 18, wherein each of the node control processors further comprises a microprocessor connected to the TSI and the ATM access controller.

31. The system of claim 30, wherein each of the node control processors further comprises a data link and control tone card (DCT) connected to the microprocessor.

32. A scalable digital loop carrier system capable of providing voice, video and data communications, the system comprising:

(a) a primary channel bank;

(b) an asynchronous transfer mode (ATM) interface connected to the primary channel bank;

(c) a time division multiplex (TDM) interface connected to the primary channel bank; and

(d) at least a first secondary channel bank connected to the primary channel bank through the ATM and TDM interfaces, wherein the primary channel bank and the secondary channel bank each comprise:

(i) a time slot cross-connect interchanger (TSI) having a plurality of subscriber bus interfaces;

(ii) an ATM access controller connected to the TSI, the ATM access controller having a plurality of ATM cell bus interfaces; and

(iii) a timing generator to provide timing reference to the TSI and the ATM access controller, the timing generator in the primary channel bank having a timing reference input and a clock synchronization output connected to provide clock synchronization to the timing generator in the secondary channel bank.

33. The system of claim 32, wherein the primary channel bank further comprises a synchronous transport signal (STS) cross-connect controller connected to the TSI in the primary channel bank.

34. The system of claim 33, wherein the primary channel bank further comprises a synchronous optical network (SONET) framer connected to the STS cross-connect controller in the primary channel bank.

35. The system of claim 33, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the primary channel bank.

36. The system of claim 32, wherein the secondary channel bank further comprises a synchronous transport signal (STS) cross-connect controller connected to the TSI in the secondary channel bank.

37. The system of claim 36, wherein the secondary channel bank further comprises a synchronous optical network (SONET) framer connected to the STS cross-connect controller in the secondary channel bank.

38. The system of claim 36, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the secondary channel bank.

39. The system of claim 32, wherein the TDM interface is capable of supporting 16 time division multiplexed channels.

40. The system of claim 32, wherein the ATM interface is capable of transporting 216 ATM cells per 125 μs frame.

41. The system of claim 32, wherein the TDM interface is capable of providing a plurality of synchronous transport signal-one (STS-1) channels in a synchronous optical network (SONET) frame.

42. The system of claim 32, wherein the timing reference input of the timing generator in the primary channel bank comprises a synchronous optical network (SONET) timing reference input.

43. The system of claim 32, wherein the timing reference input of the timing generator in the primary channel bank comprises a T1 timing reference input.

44. The system of claim 32, wherein the timing reference input of the timing generator in the primary channel bank comprises a building integrated timing supply (BITS) input.

45. The system of claim 32, further comprising a second secondary channel bank connected to the primary channel bank through the TDM and ATM interfaces.

46. The system of claim 45, wherein the second secondary channel bank is connected to the first secondary channel bank through the TDM and ATM interfaces.

47. A scalable digital loop carrier system capable of providing voice, video and data communications, the system comprising:

(a) a primary channel bank;

(b) an asynchronous transfer mode (ATM) interface connected to the primary channel bank;

(c) a time division multiplex (TDM) interface connected to the primary channel bank; and

(d) a plurality of secondary channel banks connected to the primary channel bank through the ATM and TDM interfaces, wherein the primary channel bank and the secondary channel banks comprise respective timing generators and respective node control processors,

wherein the timing generators are capable of providing clock signals for the respective channel banks, the timing generator in the primary channel bank having a timing reference input and a clock synchronization output connected to provide clock synchronization to the timing generators in the secondary channel banks, and

wherein the node control processors each comprise:

(i) a time slot cross-connect interchanger (TSI) having a plurality of subscriber bus interfaces;

(ii) an ATM access controller connected to the TSI, the ATM access controller having a plurality of ATM cell bus interfaces;

(iii) a synchronous transport signal (STS) cross-connect controller connected to the TSI; and

(iv) a synchronous optical network (SONET) framer connected to the STS cross-connect controller.

48. The system of claim 47, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the primary channel bank.

49. The system of claim 47, further comprising a plurality of STS transport cards connected to the STS

cross-connect controller in the secondary channel banks.

50. The system of claim 47, wherein the STS cross-connect controller is capable of supporting at least 12 STS-1 channels.

51. The system of claim 47, wherein the TDM interface is capable of providing a plurality of synchronous transport signal-one (STS-1) channels in a synchronous optical network (SONET) frame.

52. The system of claim 47, wherein the timing reference input of the timing generator in the primary channel bank comprises a synchronous optical network (SONET) timing reference input.

53. The system of claim 47, wherein the timing reference input of the timing generator in the primary channel bank comprises a T1 timing reference input.

54. The system of claim 47, wherein the timing reference input of the timing generator in the primary channel bank comprises a building integrated timing supply (BITS) input.

55. The system of claim 47, wherein each of the node control processors further comprises a microprocessor connected to the TSI and the ATM access controller.

56. The system of claim 55, wherein each of the node control processors further comprises a data link and control tone card (DCT) connected to the microprocessor.

ABSTRACT

A scalable digital loop carrier system uses a stackplane architecture which allows the transport capacity of the scalable digital loop carrier system to be flexibly expanded while providing time division multiplex (TDM) and asynchronous transfer mode (ATM) data link channels. The primary channel bank is provided in the scalable digital loop carrier system, and one or more secondary channel banks are connected to the primary channel bank through the stackplane ATM and TDM data links. The scalable digital loop carrier system is expandable by adding secondary channel banks to the system through the stackplane TDM and ATM data links.

Separator Sheer

III

Miscellaneous Material Includes:

1. Drawings
2. Oath or Declaration
3. Foreign language specification
4. Sequence listing
5. Computer listing
6. Appendices

Version 2.2C

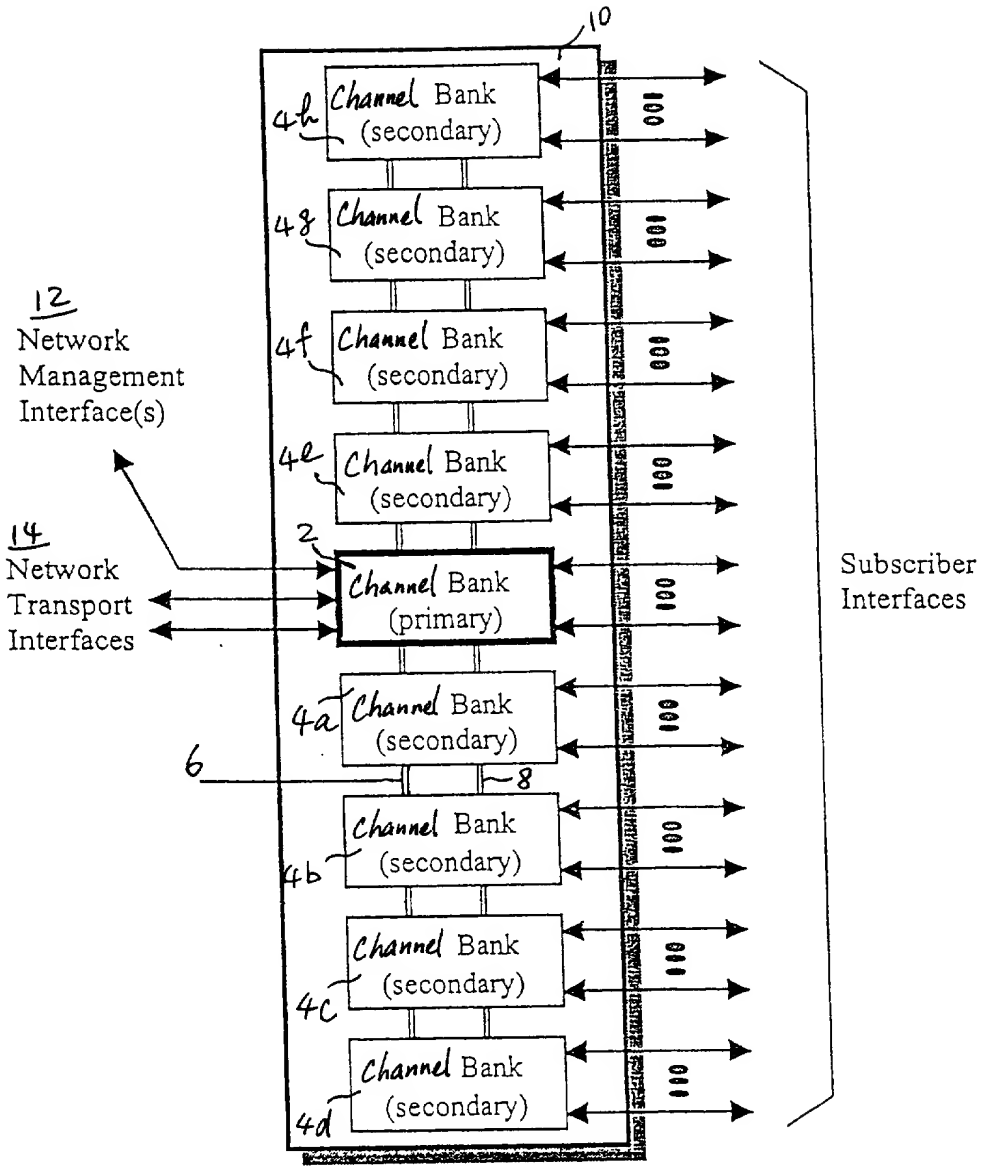

10
Channel Bank (secondary)
4h
Channel Bank (secondary)
4g
Channel Bank (secondary)
4f
Channel Bank (secondary)
4e
2
Channel Bank (primary)
Channel Bank (secondary)
4a
6
8
Channel Bank (secondary)
4b
Channel Bank (secondary)
4c
Channel Bank (secondary)
4d
12
Network Management Interface(s)
14
Network Transport Interfaces
Subscriber Interfaces

FIG. 1

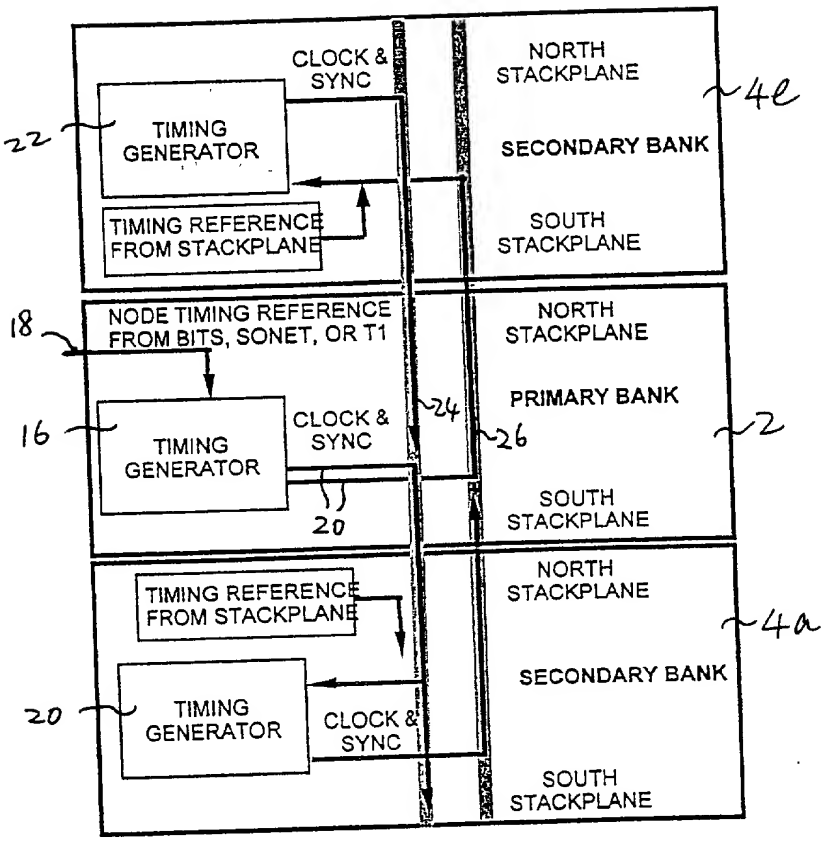

CLOCK & SYNC
NORTH STACKPLANE
4e
22
TIMING GENERATOR
SECONDARY BANK
TIMING REFERENCE FROM STACKPLANE
SOUTH STACKPLANE
18
NODE TIMING REFERENCE FROM BITS, SONET, OR T1
NORTH STACKPLANE
PRIMARY BANK
24
26
16
TIMING GENERATOR
CLOCK & SYNC
2
20
SOUTH STACKPLANE
TIMING REFERENCE FROM STACKPLANE
NORTH STACKPLANE
4a
SECONDARY BANK
20
TIMING GENERATOR
CLOCK & SYNC
SOUTH STACKPLANE

FIG. 2

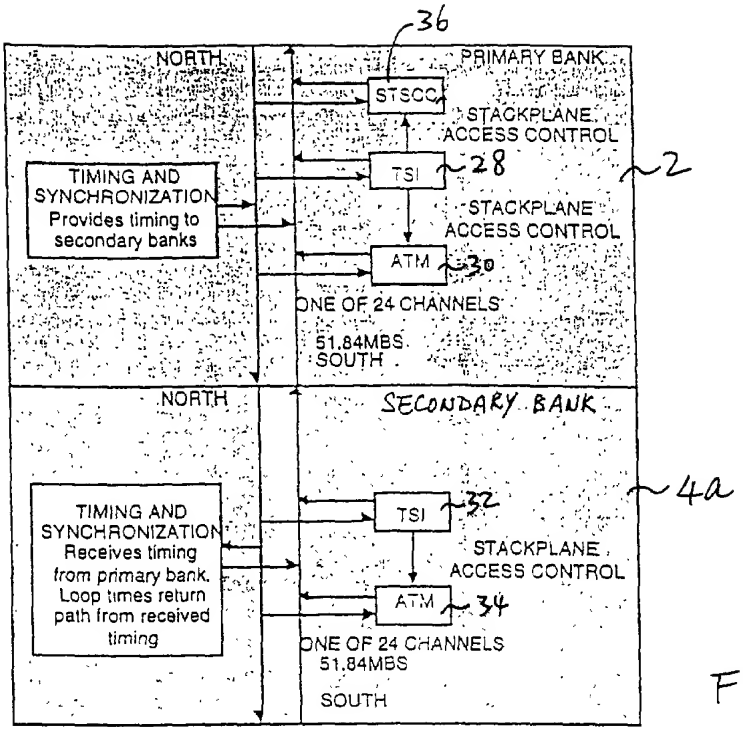


FIG. 3

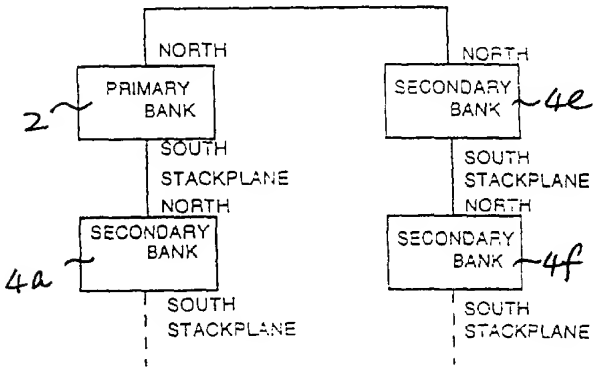


FIG. 5

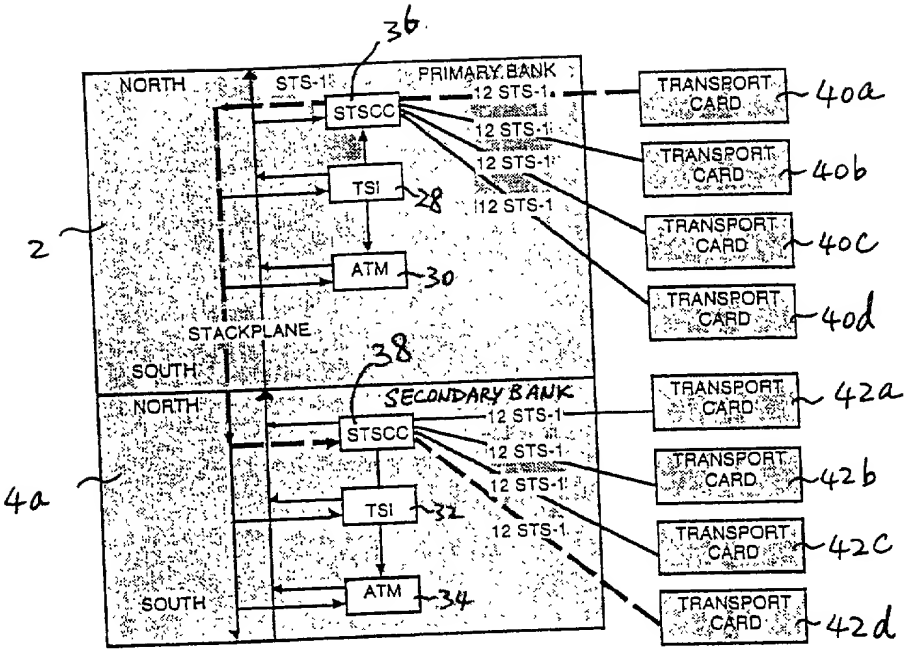

36
NORTH
STS-1
PRIMARY BANK
STSCC
12 STS-1
12 STS-1
12 STS-1
12 STS-1
TSI
28
ATM
30
2
STACKPLANE
SOUTH
38
SECONDARY BANK
NORTH
STSCC
12 STS-1
12 STS-1
12 STS-1
12 STS-1
TSI
32
ATM
34
SOUTH
4a
TRANSPORT CARD
40a
TRANSPORT CARD
40b
TRANSPORT CARD
40c
TRANSPORT CARD
40d
TRANSPORT CARD
42a
TRANSPORT CARD
42b
TRANSPORT CARD
42c
TRANSPORT CARD
42d

FIG. 4

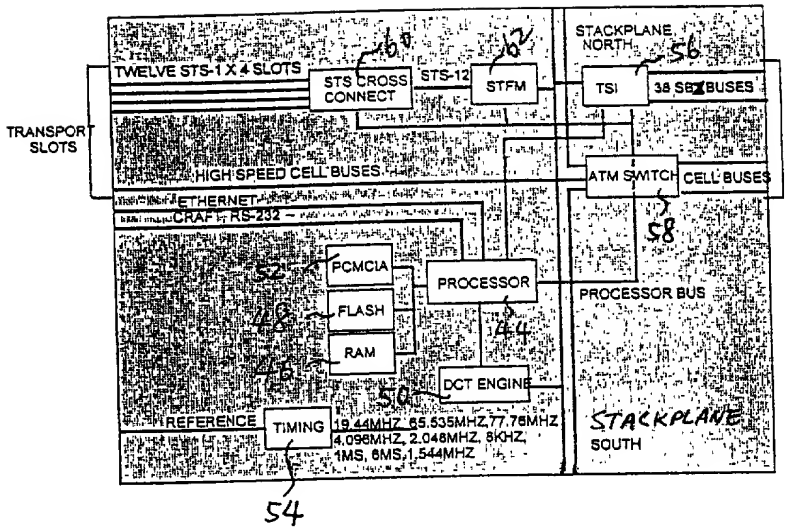

TWELVE STS-1 X 4 SLOTS
STS CROSS CONNECT
STS-12
STFM
STACKPLANE NORTH
TSI
38 SBI BUSES
TRANSPORT SLOTS
HIGH SPEED CELL BUSES
ATM SWITCH
CELL BUSES
ETHERNET
CRAFT RS-232
PCMCIA
FLASH
RAM
PROCESSOR
PROCESSOR BUS
DCT ENGINE
REFERENCE
TIMING
19.44MHZ, 65.535MHZ, 77.76MHZ
4.096MHZ, 2.048MHZ, 8KHZ,
1MS, 6MS, 1.544MHZ
STACKPLANE SOUTH
60
62
56
58
52
48
46
44
50
54

FIG. 6

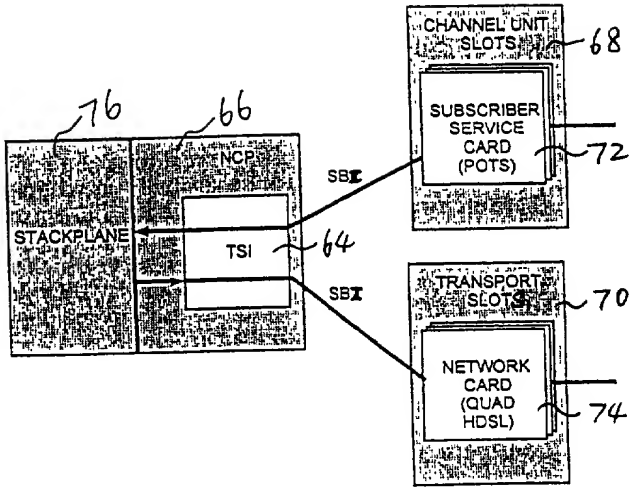

CHANNEL UNIT SLOTS
68
SUBSCRIBER SERVICE CARD (POTS)
72
76
66
NCP
SBI
STACKPLANE
TSI
64
SBI
TRANSPORT SLOTS
70
NETWORK CARD (QUAD HDSL)
74

FIG. 7

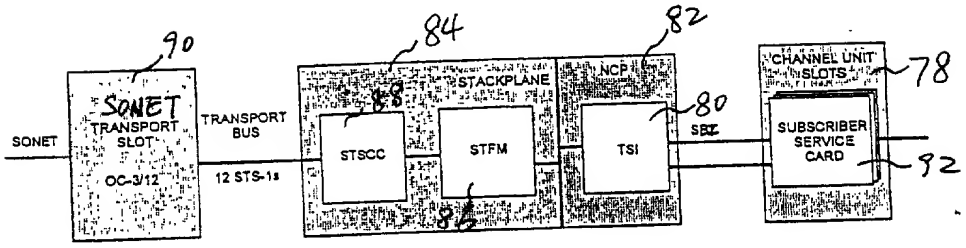

90
84
82
SONET
TRANSPORT SLOT
OC-3/12
SONET
TRANSPORT BUS
12 STS-1s
STACKPLANE
STSCC
STFM
NCP
TSI
80
SBI
CHANNEL UNIT SLOTS
78
SUBSCRIBER SERVICE CARD
92

FIG. 8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application		) PATENT APPLICATION
Inventor(s):	Jason Dove, et al.	)
SC/Serial No.:	Unknown	)
Filed:	Herewith	)
Title:	STACKPLANE ARCHITECTURE	)

COMBINED DECLARATION AND POWER OF ATTORNEY
FOR UTILITY PATENT APPLICATION

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; I believe that I am the original, first and sole inventor (if one name is listed below), first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

STACKPLANE ARCHITECTURE

the specification of which (check applicable ones):

__X__ is attached hereto;

_____ was filed with the above-identified "Filed" date and "SC/Serial No."

_____ was amended on (or amended through) __.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose information which is material to the examination of the application in accordance with Title 37, Code of Federal Regulations, §1.56.

Power of Attorney

I (we) hereby appoint WARREN S. WOLFELD, Reg. No. 31,454; SLADE E. SMITH, Reg. No. 37,447; LEE HSU, Reg No. 39,716; and other attorneys of FLIESLER, DUBB, MEYER & LOVEJOY LLP, located at Four Embarcadero Center, Fourth Floor, San Francisco, California 94111, telephone (415) 362-3800; and WAYNE A. JONES, Reg. No. 30,761; RICHARD A. MYSLIWIEC, Reg. No. 40,098; CRAIG A. HOERSTEN, Reg. No. 38,917; JOSEPH E. ROGERS, Reg. No. 33,031; V. LAWRENCE SEWELL, Reg. No. 22,753; and other attorneys of ALCATEL USA, located at 1000 Coit Road, Plano, TX 75075-5813, telephone (972) 519-3465, as my (our) attorneys, with full power of substitution and revocation, to prosecute this application and transact all business in the United States Patent and Trademark Office connected herewith.

Attorney Docket No.: DSCC1067WSW/LAH
lah/dscc/1067.004

Client Case No. 1068-00

Express Mail No EL080529871 US

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Please address all correspondence to:

ALCATEL USA
1000 Coit Road, MS LEGL2
Plano, Texas 75075

Please direct all telephone calls to:

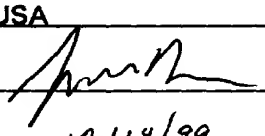
Lee Hsu, Esq.
(415) 362-3800

(1) Full name of sole or first inventor: Jason Dove

(1) Residence: 10 Jeffrey Court
Novato, CA 94945

(1) Post Office Address: same as above

(1) Citizenship: USA

(1) Inventor's signature: 

(1) Date: 12/14/99

****

(2) Full name of second joint inventor: Paul Franceschini

(2) Residence: 1485 Magnolia Avenue
Petaluma, CA 94952

(2) Post Office Address: same as above

(2) Citizenship: USA

(2) Inventor's signature: 

(2) Date: 12.14.99

Title 37. Code of Federal Regulations, §1.56

SECTION 1.56. DUTY TO DISCLOSE INFORMATION MATERIAL TO PATENTABILITY

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98.* However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office; or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

* §§1.97(b)-(d) and 1.98 relate to the timing and manner in which information is to be submitted to the Office.

****